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Detached Crystal Growth by VDS: Fabrication and Characterization of the P-N Junction, Photo and Thermo Device on the Sb-Based Substrate to Operate at the Ambient Temperature

*D. B. Gadkari,
Freelance Research & Consultant: Crystal Growth and Crystal Technology,
Embee-10A, Saibaba Nagar, Borivali (W), Mumbai-400092 India
Corresponding Author: D. B. Gadkari

Abstract: *The ultra-high quality* antimonide (*Sb) based substrates with a low dark current is prerequisite in the third generation Infrared (IR) devices. Novel strategy of the unidirectional growth for Sb-based crystals have been carried in a vertical furnace under detached conditions to reduce the buoyant thermo-gravitational convection using vertical directional solidification (VDS). In view of the traditional growth process, disadvantages of the large dark current should be removed to enhance electron carrier lifetime. Despite technology advantages of IR-devices, suppressed generation-recombination (g-r), Shockley-Read-Hall (SRH), Auger recombination, reduced tunneling, and surface leakage currents have been not revealed. First time at the ambient temperature, low dark current achieved by design and fabrication of junction devices on the substrates from the Sb-based detached crystals. Analyses for the low dark current in the p-n junction, photo and thermo device experiment have been reported for former recombination process and the superiority has been compared with the result of existing InSb devices.*

Keywords: *Semiconductors III-V, Directional solidification, detached crystal growth, Sb-based crystals, Low dark current, Doping, IR-devices.*

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I. Introduction

The narrow gap Sb-based materials have a potential in third generation IR photon detectors and integrated circuit (IC) should have high speed and low power consumption for the evolution of high-frequency HEMT and HBT transistors. The Sb-based materials have been opened new novel device research [1], these optoelectronic devices demands large size and high quality substrate for the devices yield. The space grown crystals have high quality because of the eliminated buoyant thermo-gravitational convection [2]. A comprehensive survey of detached crystal growth in orbital space shuttles have been discussed by the NASA Skylab mission-III, IV-1974 [3]. In International Space Station (ISS), the space experiments have been performed to get highest quality crystals. Further, it was proposed to use the space technology to grow detached crystal in terrestrial lab on Earth. A new epi-InSb technology has been developed to reduce the dark current due to the g-r process so that InSb detector from 80K should function in the range of 95-100K [4]. A low dark current and high quantum efficiency devices have been proposed by XB_nn and XB_pp barrier detectors fabricated on GaSb substrates. These detectors are operated up to 175K, higher than the g-r limited InSb photo-detectors at 80K [5]. The crystal growth and crystallinity of Sb-based materials is related to the defects and decreased quality with deleterious effects on the functioning of the electrical and optical IR devices [6]. The camera based on InSb sensors, the high thermal sensitivity and favorable atmospheric transition used in the 3-5μm spectral region as the traditional application. Devices certain advances : i) the passivation of InSb focal plane arrays (FPA) to eliminate surface states and to retain charge of the detector when exposed to high energy photon, i.e. the possibility after-images and image lag issue for InSb sensors [7]. ii) Thermo-electric materials have attracted attention during the last decade to convert thermal energy into electricity [8]. iii) Recently, the Sb-based materials doped by Tl, Bi, N and Te are alternative to HgCdTe and CdZnTe for IR devices to operate at an ambient temperature [1]. iv) An advantage of InSb IR detectors cooling and design of system has resulted in a new generation IR-camera in critical SWIR. v) The understanding of I-V curve to acquire device basic parameter information about the dark current mechanism has been reported for LWIR photodiode for HgCdTe [9]. In this research, the Sb-based substrates have been used which grown the detached crystal by VDS (InSb/GaSb and doped InSb/GaSb [10]. Detachment shows the high-grade physical properties of Sb-based (substrates) crystals grown ever. Eliminating adverse effect of g-r, Auger, SRH, short carrier lifetime, and

surface recombination would improve devices quality [11]. First time substrates (detached crystal) have been used for the p-n diode, photo and thermo-conducting device. Analyses of suppression or elimination of former adverse effect on performance at elevated temperature, and Sb-based devices as the substitute for HgCdTe will be reported.

II. Experiments

II.1 Sb-based substrates from the detached crystals

Devices have been designed and fabricated on the p-type and n-type InSb substrate from detached crystal grown by VDS. A p-n junction by i) Diffusion, ii) Ion implantation, iii) Vacuum evaporation, and iii) e-beam, the photo and thermo-conducting effect also on the InSb:Bi and InSb:N have analyzed. Typical physical properties of the InSb substrate is given in "Table-1", the substrate is from detached crystal grown in VDS.

II.2 Diffusion: p-n junction

In diffusion process, n-type layer on p-type InSb substrate was formed; p-type InSb substrate and Te (1.5mgrm) were kept apart inside the quartz tube (d=10mm and L=100mm). Samples were sealed in a vacuum (10^{-5}torr), then kept in a furnace for diffusion at 350^0C for one hour. For metallization, the AuZn on p- type and AuGeNi on n-type side of substrates were done in vacuum evaporation. Samples were alloyed at the 200^0C for one minute in high purity hydrogen flow, then processed by photolithography (Karl Suss MJB-3) for a mesa junction of the 500µm diameter mask on n-type substrate. A positive photo-resist (AZ1350) was used as mask to form mesa patterns of the 500µm diameter. Wafers were etched in HCl: Hf: H_2O:: 1:1:1 with an etching rate 0.25µm/min to form mesa of 3µm depth. Depth profile was determined by DEKTEK; silver epoxy was used on n-type for the connection of gold wire. The p-n junction devices fabricated by the diffusion method were isolated into individual diode and mounted for I-V measurements Fig-1a, b. Similar procedure was used for the p-type substrates. For I-V measurements, the set up of Lock-in-Amplifier, SR 530 and Keithly 617 programmable Electrometer were carried at the Research Institute Mumbai, India.

II.3 Ion implantation: p-n junction diode

I) For ion implantation study, n-type InSb substrates were used, substrate physical data : the samples size 10x10x0.3mm^3, complex InSb sample (p~n- type InSb), carrier concentration ~ 2x10^{16} to 1.8x10^{17}, mobility ~ 6.0-1.2x10^{4}cm^2/Vs, FWHM ≤ 100 acrsec, and dislocating density ≤ 10^3cm^2. The p–n junction formed by ion-implantation at a dose of 2×10^{13} 30KeV Te+ cm^{-2} and by ion-implantation at a dose of 1.8×10^{14} at 30KeV Te+ cm^{-2}. Samples were annealed at the 27^0C (RT), 100^0C, and 200^0C using convectional annealing process for the 10minute.

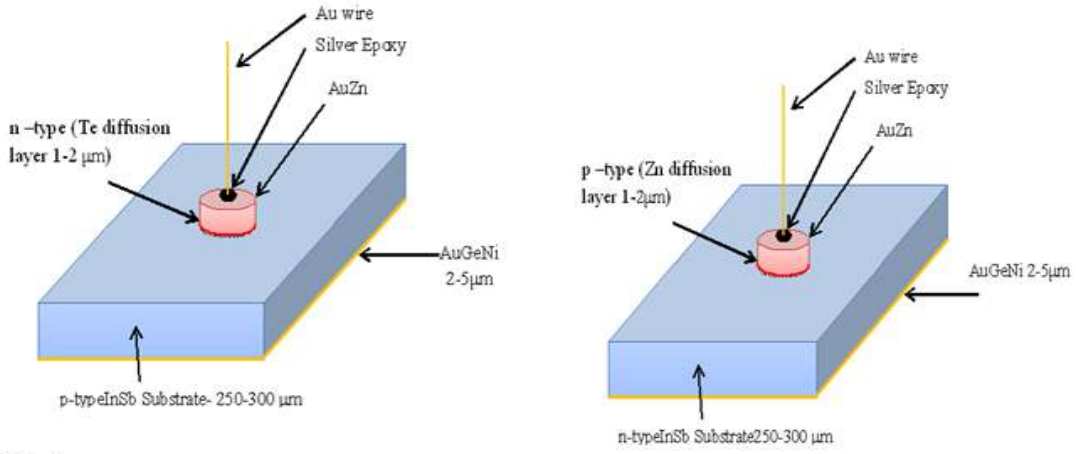

Figure 1. Schematic junction formation process on the p-type and n-type InSb substrates are shown in a) and b).

II) Boron implantation was carried out using negative ion acceleration; The beam size was 5mm x 6mm; Boron implantation dose of ions was 10^{17} cm^{-3} for the ion current 300nA to 450 nA. The wafer was not annealed to avoid further boron diffusion in the wafer. Depth of implanted ions was estimated using Stopping and Range of Ions in Matter (SRIM) software. The simulation indicates the ion range in InSb:N was 2014A where the atoms straggled about 950A for 100KeV. The distribution of ions was not uniform over depth for single stage ionization, thus two step ion implantation was carried out by an energy of ion beam in the second implantation was 50KeV. Simulated range for 50KeV was 1224A. Measurements and ion implantation were carried out at the IUAC New Delhi, India.

II.4 Thermal and Photoconductive effect

Thermal conductivity effect on the substrate by varying the temperature of heat rod (hot), photoconductive measurement on InSb:Bi (InSb:N) using monochromatic laser beam are shown in Fig-2a, b (p-type and n-type substrates). These characterization shows the purity and crystalline quality of the substrate. It is quite clear that these effects response have related to the high quality and physical properties of the crystals. In these effects, crystal purity and crystallinity is imperative. These effect result confirm that the crystals grown by VDS are highest quality.

III. Results And Discussion

VDS research experimental novel results have been published first time for the substrates from detached ingot. References were checked in literature for the similar research results to compare but did not find. At the onset substrate physical properties of detached crystals VDS were enhanced in comparison to literature reports "Table-1".

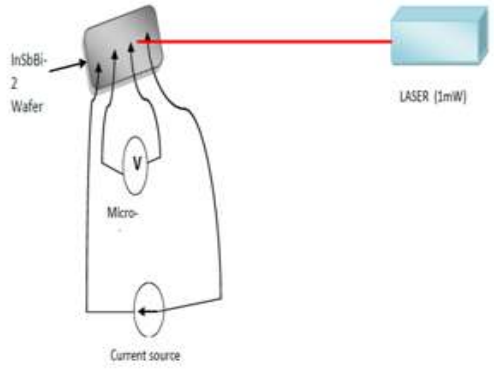

Fig-2a

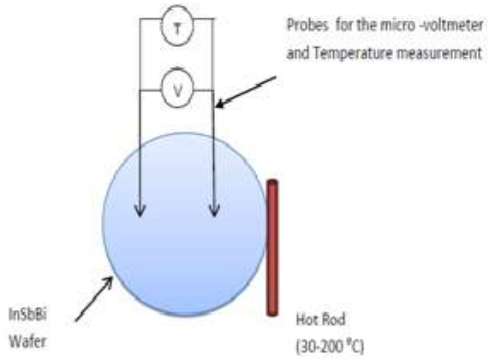

Fig-2b

Figure 2. a) Variation of resistivity by the incident LASER beam on n-type InSb:Bi substrate, b) Measurement of the Seeback effect on InSb:Bi n-type substrate.

In this research, analysis has been performed in view of i) Low dark current for high efficiency, ii) Dark current mechanism iii) Tunneling by the band to band (BTB), iii) Traps assisted tunneling (TAT), iv) SRH effect, v) g-r process, vi) Auger process for the minority life time, vii) Suppression of a leakage current, viii) Majority diffusion current, ix) Minority diffusion current, x) Surface leakage currents. From the literature survey, the dark current in a photodiode has been shown by the distinctive current components by the following equation-1

$$I = I_D + I_{DS} + I_G + I_{GS} + I_S + I_T \qquad 1$$

Where currents are - I_D: Bulk diffusion, I_{DS}: Surface diffusion, I_G: Bulk generation-recombination, I_{GS}: Surface generation-recombination, I_S: Shunt current and I_T: Tunneling current, respectively. Dark current consists of i) Bulk diffusion current by thermal generation-recombination (g-r) process in the substrate (inhibited at low temperature), ii) Surface diffusion by the similar bulk diffusion along a surface, iii) Bulk g-r current caused by the traps in the depletion region due to the shallow states for carriers, iv) Surface g-r current by the traps on the surface v) Shunt as an ohmic current with the linear I-V relationship (the surface leakage along edges or grain boundary or defects caused by metallization), vi) Tunneling current or traps assisted tunneling current appears at high reverse bias, carriers tunnel from valence band to the conduction band (band to band tunneling or the presence of traps in the band gap, vi) Small reverse bias, bulk g-r and shunt current are dominant, vii) High reverse bias, tunneling current dominant, viii) At low temperature, InSb photo detector has bulk diffusion, surface diffusion, surface g-r currents.

III.1 p-n Junction diode

The ideal physics involved in the p-n junction barrier diode (JBD), photo and thermo conductivity process are explained in brief. In the JBD device, current is carried by the majority and minority carriers. Therefore, the ideal forward bias current of a diode is expressed by a simple equation -2

$$I_D = I_S \left(e^{(qVD/\eta KT)} - 1 \right) \qquad 2$$

Where, I_D; diode current, I_S: diode saturation current, T: Absolute temperature, q: Elementary charge, k: Boltzmann constant, η: Ideality factor, V_D: Applied voltage drop on the junction. In addition the current

flows, the effect of resistance is a series combination of a diode resistance (Rd) and a series resistance (Rs), thus R = Rd + Rs. The ideality factor (η) can be expressed as in equation-3

$$\eta = (q/KT)\ 1/slope \qquad 3$$

Where, slope is from the log I-V plot of the diode characteristics at ambient temperature. Moreover, the series resistance (Rs) through the current flows can be expressed as in equation-4.

$$Rs = (KT(\gamma-\eta))/qI \qquad 4$$

Where, γ is an integer (dimensionless) γ > η. In particular, JBD parameter changes with a temperature and a bias voltage. As per reference cited in literature, there are limited literature on the properties of ion implantation (Te/n-InSb) and diffusion (Te/p-InSb). Therefore, a main aim of this research work is to investigate the electrical properties of these junctions.

Ion implantation: Forward bias (FB): The p-type InSb:Te current–voltage I-V curve, i.e. VDS-diode (equation-2) is shown in Fig-3a, b. Also, it shows the linear and Semi-log I-V curves for the ion implanted (Te) Fig-3a, b. I-V curves in Fig-3a, b reveal that the ideality factors (η) (equation-3) are 1.1, 1.21, and 1.15 for the as deposited, annealed at 100^0C, and 200^0C for 10 minutes respectively. However up to 200^0C, VDS-diode shows a correspond decrease in the rectification with an increase in a barrier height (BH). The effect of annealing on the ideality value, analysis showed that the ideality factor η = 1.1 for a sample annealed at 200^0C. For further analysis, a typical p-n JBD junction, the series resistances are measured for the forward bias at 0.2V. The observation in the n-InSb:Te VDS-diode shows the large series resistance (equqtion-4) at ambient temperature (RT). The as deposited curve showed lowest current in reverse bias with near unity ideality factor.

Table-1 the substrates specification at 300K for detached InSb ingots used for the VDS-diode

SrNo	Property of substrates	Value	Sr No	Name of property	Value
1	Substrate dimension	10x10x0.3 cm^3	8	Preferential direction	(220)
2	Mobility (μ)	$6.05x10^4$ cm^2/V.sec	9	Carrier concentration (n)	~ $3.8x10^{16}cm^3$
3	Resistivity (ρ)	$3.0x10^{-3}$Ω-cm	10	Energy band gap (Eg)	~ 0.16eV
4	Cut-off (λ)	~ 7.3μm	11	Each pit density (EPD)	~10^3 cm^{-2}
5	FWHM	~ 65 arcsec	12	Micro-Hardness (H_v)	~2.2GPa
6	I-V measurements in the temperature range	20-300K	13	Ingots dimension	L = 65-75mm d = 10-24mm
7	InSb ingots grown by VDS	35	14	GaSb ingots grown by VDS	37

Total ingots grown: 72, the vertical growth furnace (VDS) was equipped with the optimized growth conditions, parameters, growth rate, pulling down and crystal rotations. VDS system have been used to grow bulk detached crystal of InSb:Te, InSb:Bi, InSb:N, GaSb:Se, GaSb:Mn, GaSb:Mg GaSb:Bi. First time, the substrates of detached crystals have been used for the IR-devices and typical substrate has complex conduction (p-type up to~125K and n-type above), results published elsewhere (references also in ResearchGate).

I) forward bias (FB), series resistance at 0.2V are 2.11KΩ, 0.89KΩ, and 1.21KΩ, and **II)** reverses bias (RB), series resistances at 0.2V are 3.58KΩ, and 0.54KΩ, 0.12KΩ respectively. First case at (30^0C), curve shows weak rectifying contact with a large series resistance, while later two cases show improved rectification with the

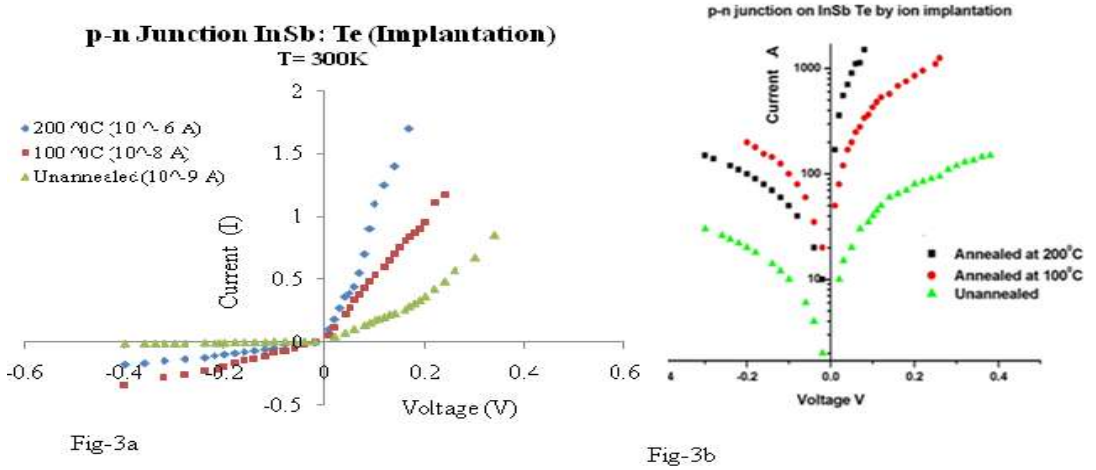

Fig-3a Fig-3b

Figure 3. I-V curves of p-n Junction formed by ion implantation on n-type InSb substrates a) linear graph and b) Semi-log graph (current scale 10^{-9}A). Dark current at RT(μA) for VDS-diode, lowest has been shown ever. increase in temperature and decrease η . In both (I, II) cases, significant difference has been measured in the series resistance and low shunt resistance in the exponential I-V curve (FB), this related to a g-r process.

Estimated current value at 0.2V for un-annealed and annealed samples RT, and 100^0C, 200^0C are 0.3nA, and 1.1nA, 1.7μA. But knee voltage decreased 0.01V, and 0.007V, 0.004V, rectifications increase (η decrease) respectively, similar in Semi-log.

Ion implantation: Reverse bias (RB): Leakage current or dark current (equqtion-2) are measured for the VDS-diode at 0.3V. The samples annealed at 200^0C have a maximum decrease in leakage current. For T > 200^0C, further increase in annealing temperature a leakage current was increased. It reveals that the defect have been generated on annealing into substrate at higher temperature. For reverse bias, as deposited samples in Fig-3a, b showed insignificant reverse current (dark or leakage current). Interestingly, it is smooth, constant with breakdown reverse voltage > -4V. It is attributed to the defect generation into the depletion layer during formation of the junction, which shows the presence of ohmic contact (high series resistance). Defect components have entered into a junction on annealing (equation-1) at 100^0C increase in g-r process. But at 200^0C (annealing), there is suppression (decreased) g-r process with a major decrease in the dark current at the ambient temperature (27^0C), measured value at -0.4V, I_r = 2uA showed low dark current in comparison to Te implantation into InSb traditional diode (substrates from conventional growths). This is attributed to the high quality crystals due to the detached growth using VDS.

Diffusion: Forward bias (FB): Measurements in Fig-4a, b at ambient temperature, the ideality factor of samples was decreased with temperature increase for RTA (t = 30 second) from 25^0C up to 200^0C. The estimated ideality factors (η equation-3) of the Te/p-InSb (diffusion) VDS-diode are 1.28, and 1.18, 1.13 and 1.1, for the diffusion sample annealed at RT (30^0C), and RTA at 140^0C, 150^0C and 200^0C respectively. With increasing temperatures, the curves removes surface adsorbents and converts the Au ohmic contacts from weakly into a strong rectifying barrier (BH) for 140^0C, 150^0C and 200^0C, however at the 200^0C temperature curves showed highest Au rectifying contacts and low ideality factor (η), near to unity. Fig-5, the series resistance are measured at RT (30^0C), and RTA at 25^0C, 120^0C, 140^0C, 150^0C, 200^0C. **I)** forward bias (FB) series resistances (equation-4) in the 0.3V are 8.7KΩ, 12.2 KΩ, 49.2KΩ, 22.9KΩ, 23.8KΩ, 18.8 KΩ and **II)** reverses bias (RB) series resistances at the 0.3V are 8.5KΩ, 14.2 KΩ, 76.9.2KΩ, 32.9KΩ, 88.2KΩ, 102 KΩ respectively. First three cases (<140^0C) showed ohmic contacts since there is no major difference in both (I, II) series resistance, but later, three cases shows the rectifying

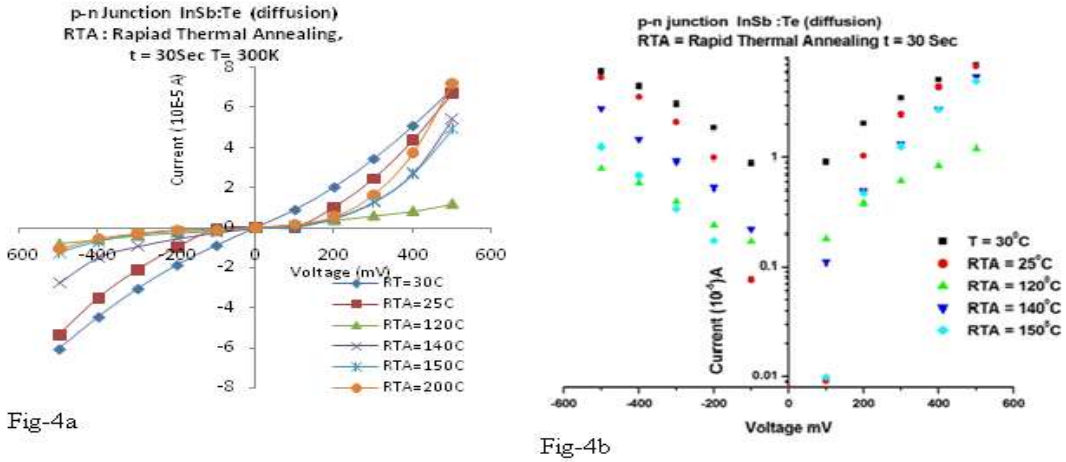

Figure 4. I-V curves for junction formed by diffusion of Te into p-type InSb substrates, a) As grown annealed sample for 10 minutes at 30^0C by conventional annealing and b) RTA method, sample annealed for 30 seconds from 25^0C up to 200^0C. The strong rectifying contact at 200^0C is seen η = 1.1. contacts, as there is a significant difference in both (I, II) series resistances, temperatures below 140^0C curves showed the weak rectification and Au ohmic contacts by series resistance and dominant g-r process (equation-1).

Diffusion: Reverse bias (RB): In VDS-diode Fig-4a, b, the leakage current of as deposited, and RTA samples are measured at 0.2V. RTA samples, the different temperatures up to 200^0C showed the decrease in leakage current at 0.2V with increase in temperature. Results indicate the electrical properties after RTA are improved an interface. In reverse bias, defects could be suppressed on annealing with the decrease in the dark current, with effect changes in the depletion regions. The defects could be introduced during ion implantation and diffusion process. The increase in reverse voltage drop at higher annealing (200^0C) in both samples may be due the reduction in g-r process (equation-1), reveals that the detached crystal has a highest crystal quality all along the growth direction (c-axis). From I-V characteristics, it is noted that the value of ideality factor greater than one/unity attributed to distribution of the interface state. The higher value of ideality factor shows the presence of a wide distribution of the interface states, and lower BH caused by the laterally inhomogeneous

interface. The performance of the VDS-diode was improved after short heat treatment (RTA). These improvements showed for the substrates of the detached crystals, i.e. the self-purification and self-passivation during detached growth process in VDS, related to the reduction of the interfacial layer and interface state densities after proper annealing. Thus enhanced electrical characteristics and boost in performance of the InSb VDS-diode. Forward bias curves, similar to the traditional InSb diode (conventional), but VDS-diode reverse bias has shown low leakage (dark) current attributed to elimination of quality affecting factors. In view of former discussions on VDS-diode - i) I-V curve (FB) represents high quality VDS-diode curves because substrates have quality, crystallinity with the increase in Barrier height (BH), ii) Series resistance of the junction depends on a doping concentration, and increases with doping, but decreases with increases temperature, iii) For strong rectification, the forward bias I-V characteristic series resistance decreases and current increases with an increase in temperature (annealing), iv) Ideality factor decreases with effect of the increase in temperature, as a result increase in BH, v) The dark current in diffusion VDS-diode is increased 20 times in comparison to the Te implantation. The diffusion at 350^0C (one hour) has introduced defects into substrates by affecting and deteriorating the substrate high quality, even though the RTA has eliminated many of the defect factors, vi) Junction posses the resistance formed by diode resistance (Rd) and series resistance (Rs), R = Rd + Rs. vii) The surface states have a major impact on electrical properties. The large value of series resistance attributed to various types of defect factors (as explained in section-3) may be initiated during the fabrication and measurement process. VDS-diode results indicate electrical properties of p-n junctions superior on annealing

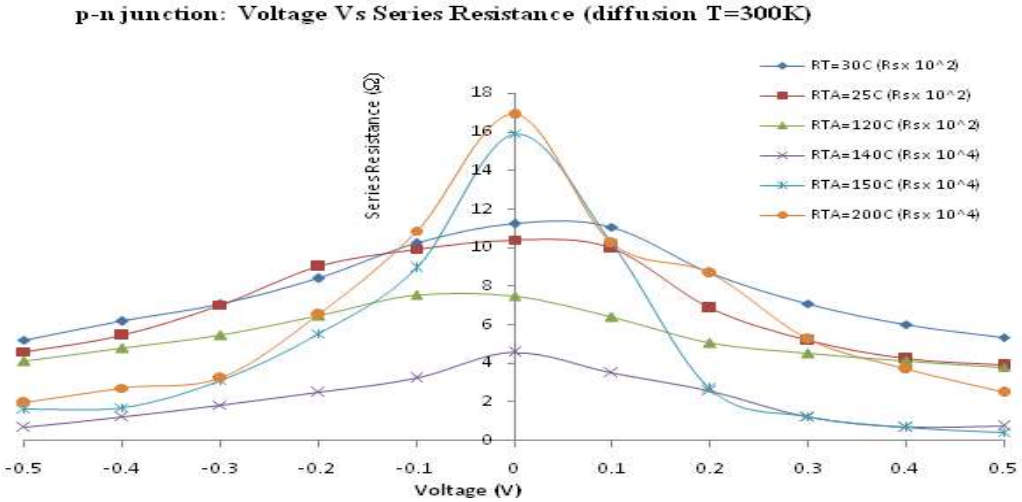

Figure 5. Rs Vs V curves, the voltage against series resistance of a p-n junction at RT. The series resistance decreases as the temperature increases. In ohmic contacts series resistance has very high value, while for rectifying contact it is very low value.

by g-r, SRH suppression / elimination, and effect in increased Auger carrier lifetime due to the smooth and uniform depletion layer (interface junction); the high quality substrate reveals superiority by suppression of the factors affecting quality in the Sb-based growths in VDS. Results reveal the reduced defect density, low reverse leakage current, lowest ideality factor and higher barrier height for VDS-diode in comparison to traditional diode, which is not operating above 80K. Thus the detached crystal growth is potentially new growth process.

III.2 Photo and Thermo-conduction

Photo-conducting effect: A photodiode is a photo-controlled current source in parallel with a semiconductor diode, and expressed by the standard diode equation-5

$$I_d = I_{dk} (e^{qVd/2KT} - 1) + I_p \qquad 5$$

Where I_d : the total current, I_p: the photocurrent, $I_{dk:}$ the dark current (leakage current), V_d : the voltage across the diode junction, q : the charge an electron, k : Boltzmann constant, T : the temperature in degrees Kelvin. At RT (T: 30^0C) Fig-6a, the current is more in the sample under illumination. It is attributed to the contribution of photo generated carriers produced upon illumination (equation-5). The photo current is very sensitive to the substrate quality. Detached Sb-based crystals have generated photo current because of the high quality growth in VDS process. The current in the InSb:Bi substrates increased as the laser source intensity increases, obviously by the large current flow of photo-generated carriers through the substrate surfaces. The series resistance should decrease with the increase in applied potential. The high defect density and low doping concentration has high series resistance. As effect may be an increase in the density of free charge carriers de-trapping mechanism by the laser energy (monochromatic beam). The presence of dark current and factors

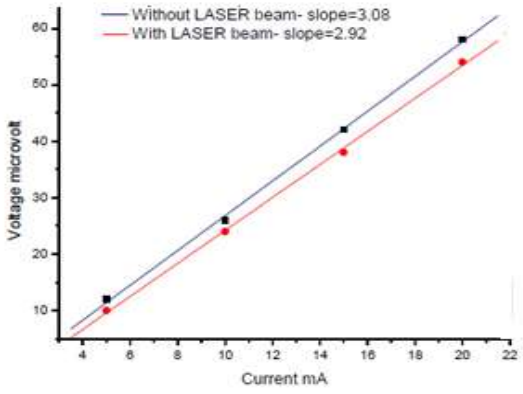

Fig-6a

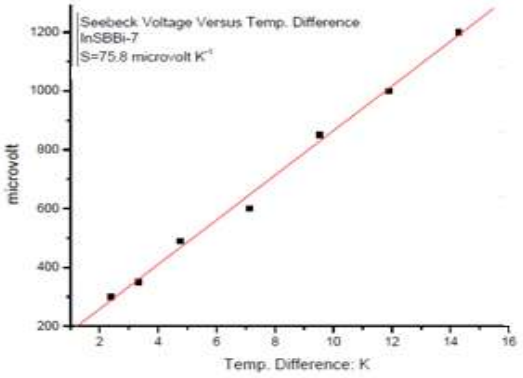

Fig-6b

Figure 6. I-V characterization of the photoconduction effect in InSb:Bi substrate showed very high response, a), the graphs shows decrease in slope on an incident beam of LASER. Thermo-conduction effect also seen in InSb:Bi substrates, Voltage Vs Temperature graph shows Seebck coefficient S = 75.8μV/K as enhanced result of crystals.

affecting the I-V characteristics of the substrates from detached ingots (high quality) are suppressed. The sensitivity to growth uniformity and its search for a focal plane array (FPA) has resulted for high quality substrates. *Thus the analysis is under process*.

In conventional growth, one of few prominent disadvantages with the technology is effect on spectral uniformity and dark current in (FPA). The present benefits from VDS, the high quality, the high growth uniformity and availability of large size substrate of the III-V material are recent requirement. However, the dark current generation dominated by thermionic process limits the competitiveness of the operating temperature and integration time. The upcoming notable detector technologies, IR photo-detectors predicated to outperform the HgCdTe (MCT), CdZnTe(CZT) II-V materials at low temperature technology of high effective mass and lower Auger generation and control on SRH (equation-1). Recent advantages of the narrow band gap Sb-based crystal (detached) has interest to investigate the photo-detector and imaging. the potential advantages of III-V are long carrier life tome, controlled SRH, suppressed Auger by high strain.

Thermo-conducting effect: The efficiency of thermo-electric devices determined by the materials dimensionless "Figure of Merit (ZT)". Generally high-quality thermo-electric material, should acquire the large Seebeck coefficient, low thermal conductivity and high electric conductivity. ZT of materials is shown in equation-6

$$ZT = (S^2\sigma/K)\,T \qquad 6$$

Where, S: Seebeck coefficient, σ: electrical conductivity, k: thermal conductivity and T: absolute temperature. At RT (300K) Fig-6b, the voltage is more in the samples under the heat source. I-T characteristics on VDS-substrates indicate that as the temperature increases the voltage across the samples also increases (equation-6). The calculated Seebeck coefficient S=75.8μV/K, it is attributed to the contribution of thermo generated carriers produced upon heat (radiation) on the samples. The increase of doping concentration in samples enhances the voltage and therefore response to temperature through the sample region is more at a larger voltage of thermo generated carriers. The series resistance in the samples decreases with the increase of temperature. This may be an increase in the number of density of free charge carriers by de-trapping mechanism, and reduced the various types of factor affecting defects, low doping concentration, and the samples have high series resistance. The presence of surface state, defects are found to be eliminated in I-T characteristics (detached growth). *Thus the analysis is under process*.

IV. Conclusion

We have investigated the potentiality of Sb-based single crystal growth of the III-V materials, and its prospects and crystal quality by the detached growth in VDS :

i) InSb substrates (detached ingot) show homogeneous p-n junction with low level of dark currents at RT (< μA) and it is attributed to the enhanced substrate crystal quality. The InSb VDS-diodes (operate at 300K) have increased BH and improvement in performance as compared to recent XB_nn and XB_pp (operate at 170K) and traditional InSb-diode (operate at 80K), because it dependent on the use substrate quality and the applied crystal growth process. Thus VDS growth is a potentially system for the high quality crystal growth.

ii) I-V characteristic, VDS-diode (detached crystal) shows low dark current at ambient temperature (300K). The operating temperature has been increased by the four times that of the traditional InSb-diode.

iii) In Sb- based substrate (detached growth), impurity damage / defect density have been suppressed with consequence of lower contribution of g-r centers than the standard InSb p-n junction. The steeper part of each current is diffusion limited current, while the less steep part is g-r limited.

iv) The Sb-based substrates (detached) show significant improvement in longer carrier life time (SRH and Auger suppression) and proposed successful replacement to traditional MCT, CZT (operate at Low temp.)

v) The g-r current arises from the SRH is attributed to traps or native defects in the depletion interface layer. The long Auger life time (minority) in VDS-diode makes promising candidates. Dark current lowered in VDS-diode is attributed to reduction in interface mesa surface leakage current or tunneling current.

vi)The Sb-based substrates showed the best response to the photo-conducting and thermo-conducting properties at the ambient temperature because of highest quality substrates (detached crystal growth by VDS).

We look forward in the future, new high performance Sb-based devices and integrated circuit will achieve on these Sb-based substrate (detached crystals) and potential applications in a wide range of important high tech fields, viz. infrared imaging technology, digital radar (multifunction system), biomedical diagnostics, mobile communication, and thermo photovoltaic power generation system.

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Dr D B Gadkari, received B Sc (Physics) degree (1974) from Shivaji University, Kolhapur and M.Sc. degree in Physics from Bombay University (1976), and then University of Mumbai confirmed M Phil (1986) and Ph. D. under UGC-FIP (1998). He joined Mithibai College, Mumbai India in Nov-1976 as a Lecturer (Asst. Professor), HOD- Physics 2000-14, and Principal (I/C) 2013-2014. Adjunct Research Guide- Faculty of Science: University of Mumbai (2014-2017). From June 1, 2017, Freelance Research & Consultant: Crystal Technology (Crystal Growth, Material Science, Solid State devices & Physics of devices). Dr Gadkari has published 46 articles in referred journals and in the 28 proceedings. Research Areas: Bulk Crystal Growth, Material Science, Electronics and Optoelectronics devices. Single crystal growth, a new growth process - vertical directional solidification (VDS) has been developed successfully using the detached growth concept for highest quality bulk crystals in a terrestrial lab, it is analogous to the crystal grown in outer orbital space craft. He was in the University of Mumbai, Board of Study Member in Physics (2005-2014), Faculty of Science Member (2005-2014); also on Board of Study Member in Bio-Physics (2010-2014). Dr Gadkari is on body / member of professional International and National referred research journals. He has successfully completed Research projects (nine) sponsored by government and parent institute. Two Indian patents in his name for detached crystal growth by VDS in the terrestrial lab (on Earth). This research approach has opened a new area for high quality entire detached single crystal growth of Semiconductor materials.

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